

FPGA assignment: student starter

Copy each code listing into a plain-text file with the filename shown. In LabsLand, use **leds_mirror.v** for the module source.

leds_mirror.v (student starter)

```
// Copy into leds_mirror.v in the DE1-SoC Verilog Teach profile.
// E = SW[2], A = SW[1], B = SW[0].
// TODO: replace the constant on LEDR[0] with your access-rule expression.
// This starter compiles, but intentionally DOES NOT implement the rule.
module leds_mirror(input [9:0] SW, output [9:0] LEDR);
    assign LEDR[0] = 1'b0;
    assign LEDR[3:1] = SW[2:0]; // E, A, B in switch order
    assign LEDR[9:4] = 6'b000000;
endmodule
```